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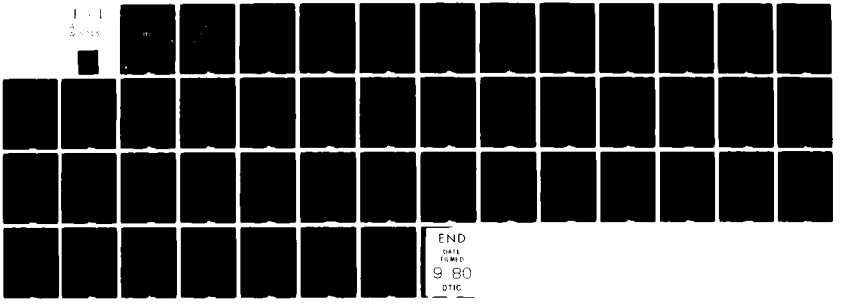

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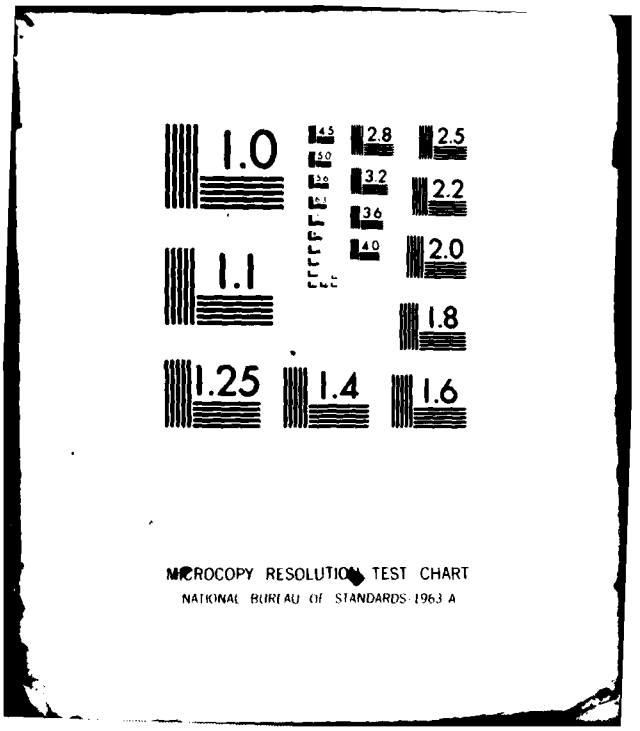
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| Trap Depths | Staircase Charging |

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The steady state current through the double dielectric of MNOS capacitors on p-silicon substrate was measured as function of temperature for several fixed fields in the silicon oxide of a polarity promoting hole flow from the silicon. It is shown that the availability of empty recipient trap states for holes tunneling from the silicon into the nitride controls the current. The occupancy of these trap states is governed by Frenkel-Poole detrapping at elevated temperatures and by Fowler-Nordheim tunnel emission from the traps at low temperature. Transient charging measurements support this interpretation.

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# CHARGE STORAGE, RETENTION AND ENDURANCE

# IN MNOS DEVICES

FINAL REPORT

Principal Investigator: Prof. K. Lehovec

Department of Electrical Engineering

UNIVERSITY OF SOUTHERN CALIFORNIA

University Park, Los Angeles, Ca. 90007

June 13, 1980

for

U.S. ARMY RESEARCH OFFICE

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Contract Monitor: Dr. Horst R. Wittmann

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APPENDIX A. "Temperature Dependence of MNOS Currents at Constant Oxide Fields"

## 1. Statement of Problem

The contract called for a theoretical analysis of charge storage and charge transfer in MNOS memory structures, and for experiments supplementing this analysis. Included in the study were predictions of charge retention, and charging experiments using constant current, rather than the customary constant voltage pulses.

## 2. Summary of Results

Just prior to the start of the project, we computed[1] transient charge distributions in the nitride based on a model which assumes:

(i) charge flow of carriers of one polarity only, entering through the oxide;

(ii) charge storage in traps of a single trap depth and uniformly distributed through the nitride.

(iii) constant current pulses and therefore constant field at the oxide/nitride interface (i.e. neglecting interface charging).

As part of the contract the same model was applied to explain experimental data on the high temperature charge retention in the nitride[2]. The experimental results show that the decrease in the threshold voltage window is initially independent of temperature, and is proportional to the logarithm of time; both features are explained by back tunneling through the oxide[3]. However, at elevated temperatures the decay of threshold voltage becomes more rapid after an incubation period which decreases with increasing temperature. This accelerated decay was explained by our model considering detrapping from traps within the nitride and drift of released carriers toward the oxide interface. Theory matched to the experiments indicates a reasonable Frenkel-Poole coefficient of $5.2 \times 10^{-4} cm^{1/2} \cdot V^{-1/2} eV$, and a trap depth of 1.5eV. Obviously, detrapping from these rather deep traps could not occur at room temperature.

Experiments on the retention loss at moderately elevated temperatures ( 154-205°C ) could not be matched by our model. Rather than invoking ad hoc additional mechanisms, we decided to extend the experimental data base so as to arrive at a better general understanding of the charge transport process in MNOS structures.

A survey of literature indicated to us that:

(a) available experimental data are almost generally inadequate, and

(b) theoretical analysis (including our own[4]) is either based on oversimplified models, or else includes so many different parameters[5] (carriers of both polarities; multitrap levels, etc,) which are clearly beyond resolution by existing experimental data.

The reason for the poor experimental data base is the intrinsic complexity of the subject, e.g.:

(a) it is characteristic of a memory device, and in particular the MNOS memory device, that the same initial state cannot be reestablished easily in a sequence of experiments.

(b) Charge transport in the MNOS Structure occurs by tunneling through the oxide barrier, and by Frenkel-Poole transport through the nitride. These two mechanisms occur simultaneously, so that it is difficult to separate them.

(c) Both mechanisms depend strongly on the electric field. Because space charges in the nitride are the basis of the MNOS memory mechanism, there is necessarily an inhomogeneous field distribution; e.g., the steady state field in the oxide is not precisely known when a D.C. gate voltage is applied.

(d) It is difficult to distinguish the charging which occurs by carriers of one polarity entering from the silicon and the charging which occurs by carriers of the other polarity entering from the gate.

Great progress in the experimental analysis of charge distribution in the nitride was made by measuring charge injected by pulses of increasing duration, each pulse being applied at the bias voltage which provides flat band (Yun method[6]). The centroid of the charge stored in the nitride can then be derived under certain conditions from change of flat band voltage and

of charge passed through the external circuit. However, the Yun method[6] requires that the sample must be restored to its initial state between pulses; the reverse polarity pulsing used to achieve this restoration may introduce carriers of the opposite polarity. Moreover, such a procedure is extremely time consuming; a single charging run over the entire range of voltage durations takes hours. Finally, the electric field in the oxide is known only at the onset of the pulse; this field decreases during the pulse in an experimentally undetermined manner.

Our principle achievement under this contract has been to devise and develop a new measurement technique[7] which eliminates all the aforementioned difficulties of the Yun method[6].

This is accomplished by charging the nitride using a sequence of identical pulses (hence "staircase charging"), thereby removing the time-consuming restoration of the initial state, and the potential complexities due to the introduction of charge of opposity polarity by reverse pulsing. Since we apply short (microsecond range) and comparatively low voltage pulses, the charge increment per pulse is kept small and oxide field and

and current remain nearly constant during a pulse. The oxide field is known from the applied bias voltage and from the oxide and nitride capacitances. Deep depletion, which would cause a significant potential drop, is prevented by the rapid build-up of inversion charge due to a pulsed laser beam impinging on the sample at the onset of the gate voltage pulse [Fig.1]. Using the computer control[8] in the feedback loop between the circuit sensing the MNOS capacitance, and the circuit adjusting the gate bias voltage to flat band, we reduce the time interval between pulses, and therefore back-tunneling. The total time for generating the experimental data for a complete charge vs.-centroid relationship is thus reduced to minutes. The data is stored in the PDP 11 computer used for the aforementioned feedback control, and is processed by the computer to provide desired relations such as will be discussed shortly on hand of Figure 2.

Since the termination of the contract, an IBM computer #5110 became available from another project, and it is now being installed as a controller for the PDP 11 which will become

a slave computer to run the experiment in a manner dictated by the IBM 5110. The IBM computer will store the data on tape, analyze it and display it graphically on an HP 9872A digital plotter.

Figure 2 shows a typical graph produced by our staircase method. The raw data are the step-wise increase in flat band voltage and in the charge passed through the oxide. The two properties derived from these data are the charging current (=charge increment divided by pulse duration), and the charging efficiency (=nitride capacitance times change in flat band voltage divided by charge increment). The centroid position divided by the nitride thickness equals one minus the charging efficiency. However, as in the Yun method, this provides the true centroid only under certain conditions (e.g. no charge crossing the nitride/gate boundary) which may not always be satisfied. As a matter of fact we attribute the decrease of charging current before the minimum (seen in Figure 2) to a reduction of charge injection through the oxide, and the increase of charging current after passing through that minimum to the injection of opposite charge from the gate[9]. The delayed injection from the gate is

due to the build-up of the gate field with increasing flat-band voltage.

Using the staircase charging method we have measured the steady state current as function of temperature and known oxide field (see Appendix). Such extensive data has never been produced before and their interpretation modifies the current model for charge injection in the trap-assisted tunnel regime: Injection of carriers from the silicon through the oxide into the nitride is not governed by the transition probability through the barrier[10] but rather by the availability of empty traps at or near the oxide nitride interface into which tunneling can take place.

Our staircase charging method and the elaborate equipment we assembled for its execution is unique, and the potential value of this tool is well recognized in the industry. This is evident from the fact that several manufacturers (Rockwell International, McDonnell Douglas and Westinghouse) have supplied us with samples for analysis by the staircase charging method. Moreover, we have obtained a short term work order from Sandia Corporation for the measurement of charge injection and steady-state current of MNOS capacitors by the staircase charging method.

Sandia will supply appropriate types and number of devices.

In summary, we have provided a new tool for the experimental investigation of MNOS memory capacitors. Application of this tool to the steady state current through the dual dielectric as function of oxide field and temperature has already lead us to modify the existing model for charging through the oxide. It is anticipated that large scale application of our method to a wide range of samples supplied by a variety of sources will generate an extensive data base from which a still more complete understanding for charge transport in MNOS structures can be derived. We are particularly eager to study the endurance phenomenon which was initially planned for this contract but which had to be postponed for lack of an appropriate experimental tool. The staircase charging method developed under this contract has now provided us with a powerful tool for this study.

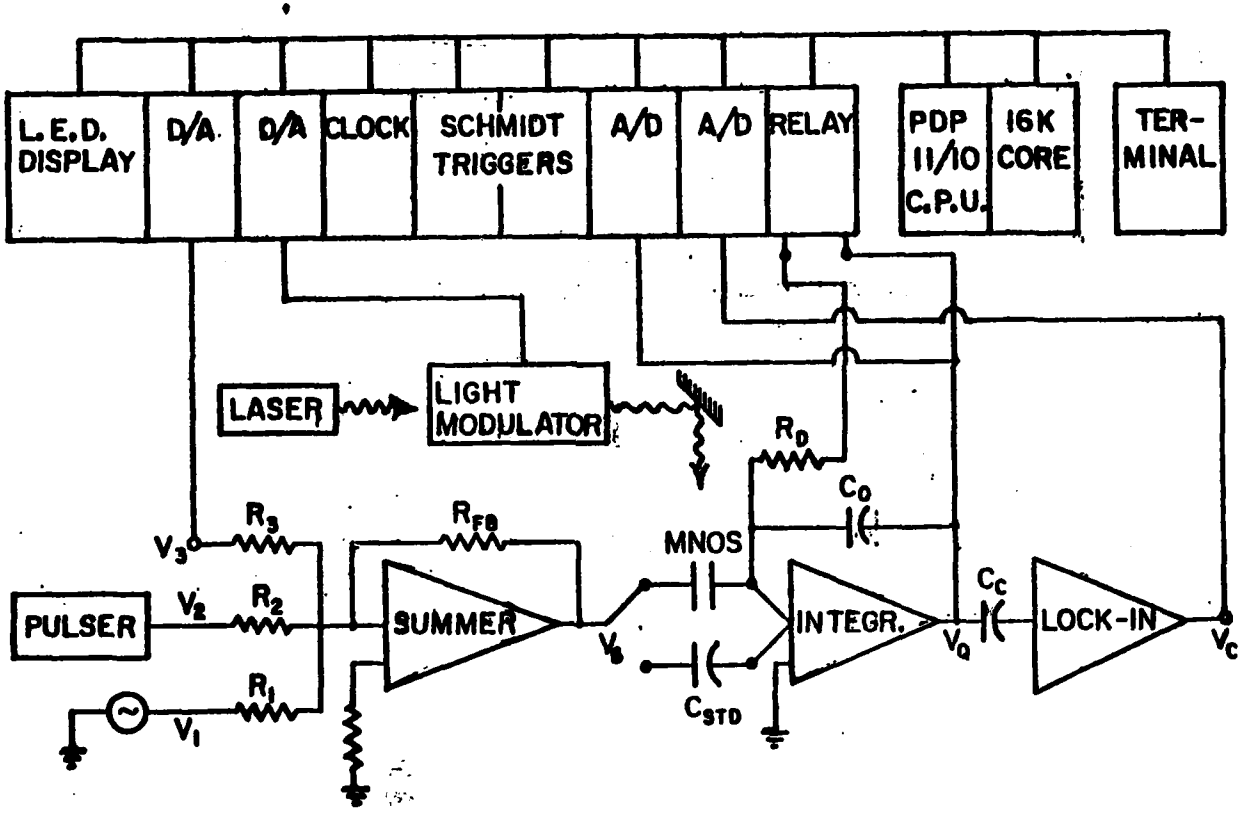


Figure 1: Computer-controlled testing circuit for staircase charging, according to ref. 8.

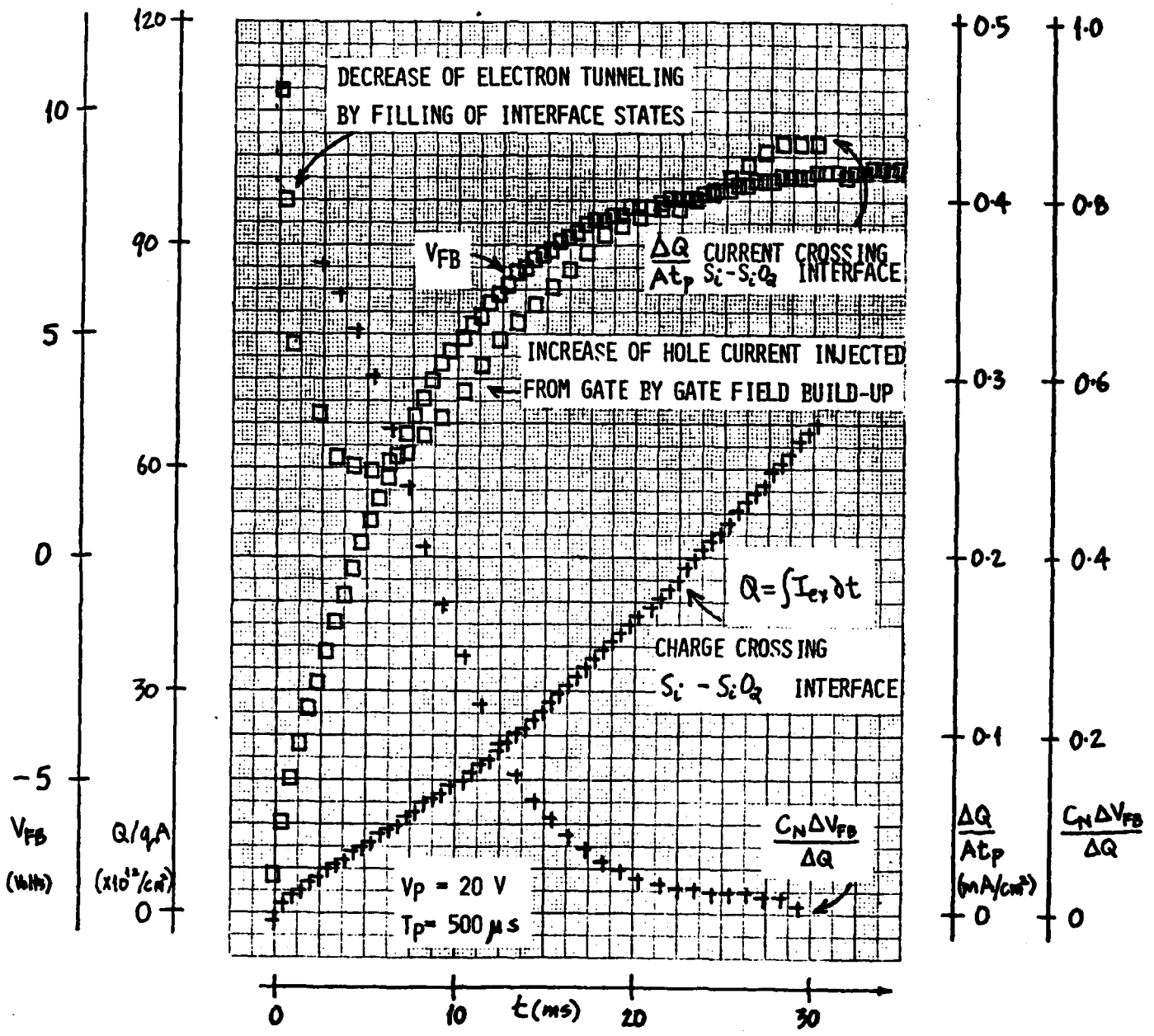


Fig. 2: Flat-band voltage and Charge Build-ups in a Staircase Charging Experiment, from which charging current and charging efficiency are derived.

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10. "Trap Assisted Charge Injection in MNOS Structures," J. Appl. Phys., 44, 4657 (1973), C. Svensson and I. Lundstrom.

LIST of PUBLICATIONS

"Charge Retention of MNOS Devices Limited by Frenkel-Poole Detrapping, Appl. Phys. Lett. 32, No. 5, March 1, 1978, pp. 335-338, K. Lehovec and A. Fedotowsky.

"MNOS Charge vs. Centroid Determination by Staircase Charging", IEEE TRans. Electron Devices, ED-25, No. 8, pp. 1030-1036 (1978), K. Lehovec, Chih-Hong Chen and A. Fedotowsky.

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"MNOS Analysis by Staircase Charging", presented at the 1979 IEEE NVSM Workshop at Monterey, Ca. March 14, 1979, K. Lehovec, A. Fedotowsky and Chih-Hong Chen.

"Mechanism for Hole Injection from p-Si through Thin Oxide Films in MNOS Structures", to be presented at the 1980 IEEE Non-Volatile Semiconductor Memory Workshop, Vail, Colorado, August 26-28, 1980; also submitted to Appl. Phys. Letters.

SCIENTIFIC PERSONNEL

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Dr. Y. Park, Post Doctoral Fellow

Chi-Hong Chen, PhD Student

Shi-Tron Lin, PhD Student

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Dr. Chen's thesis "Electrical Studies on Modern Field Effect Semi-Conductor Devices" was in part supported by this grant.

# APPENDIX A

## "TEMPERATURE DEPENDENCE OF MNOS CURRENTS AT CONSTANT OXIDE FIELDS"*

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The steady state current through the double dielectric of MNOS capacitors on p-silicon substrate was measured as function of temperature for several fixed fields in the silicon oxide of a polarity promoting hole flow from the silicon. It is shown that the availability of empty recipient trap states for holes tunneling from the silicon into the nitride controls the current. The occupancy of these trap states is governed by Frenkel-Poole detrapping at elevated temperatures and by Fowler-Nordheim tunnel emission from the traps at low temperature. Transient charging measurements support this interpretation.

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*Supported by the Army Research Office, Grant DAAG29-79-C-0095

**On leave from INHA University, INCHOEN, KOREA 160

The steady state current through the dual dielectric of MNOS devices comprises charge transport through the oxide, generally ascribed to a tunneling mechanism, followed by charge transport through the nitride, believed to be governed by some detrapping mechanism. The key measurement parameter for the oxide tunnel current is the oxide field. Measurements at constant gate voltage provide an approximate average nitride field but leave the oxide field ill-defined due to the unknown space charge distribution in the nitride. In this letter we give experimental results for the temperature dependence of the steady state MNOS current at constant oxide fields and discuss the implications of these data for MNOS device modeling.

The samples investigated by us were obtained by courtesy of R. Cricchi from the Westinghouse Corp. and had a p-type silicon substrate, an Al gate of area $A=3 \times 10^{-3} cm^2$, oxide and nitride thicknesses of $d_{OX}=22\mathring{A}$ and $d_N= 400\mathring{A}$, respectively. Application of negative gate voltage pulses resulted in a negative shift of the flat-band voltage which indicates that hole injection from the silicon dominates over electron injection from the gate.

Fixed voltage pulses $V_p$ of short duration $t_p$ in the microsecond to millisecond range applied at flat band bias voltage generate the oxide field where $C_{OX}$ and $C_N$ are the

$$E_{ox} = \frac{V_p}{A\varepsilon_{ox}} \quad \frac{C_{ox}C_N}{C_{ox}+C_N} \qquad (1)$$

oxide and nitride capacitances and $\varepsilon_{OX}$ is the permitivity of the oxide. First a large number of pulses was applied using our staircase charging technique[1,2] until a quasi-stationary state of the flat band voltage was reached. During this time period the integrating capacitor in the circuit was shunted by a resistor in order to prevent saturation of the charge amplifier. The shunt resistor was then removed using a relay, and the flat-band coltage $V_{FB}$ and the integrated charge $Q_M$ passing from the silicon into the oxide were registered after each pulse. Between pulses the gate bias voltage was readjusted to flat-band by the digitized feedback circuit described elsewhere[2]. The steady state current density $J_{ST}$ is then $Q_M / t_p A$.

Experimental Results.

Figure 1 shows the steady state current density plotted

against reciprocal absolute temperature for several constant oxide fields corresponding to the pulse voltages indicated in the figure. The current is found to be independent of temperature at low temperatures ( < -100°C ) and thermally activated at elevated temperatures. The points indecated by crosses and fitted by the dashed lines are obtained by subtracting from the observed current density $J_{ST}$ the temperature independent current $J_2$ (dotted levels at low temperatures). The activated energy is displayed in Figure 2 in a Frenkel-Poole type plot,

$$\psi = \frac{\partial \ell n (J_{ST} - J_2)}{\partial (kT/q)} \equiv \phi_T - \beta\sqrt{E_N} \qquad (2)$$

from which $\phi_T = 0.34V$ and $\beta = 1.5 \times 10^{-4} cm^{\frac{1}{2}} V^{\frac{1}{2}}$
The nitride field at the nitride/oxide boundary, $E_N = E_{OX}\, \varepsilon_{OX} / \varepsilon_N$, used in this plot disregards the interface charge.

The dashed lines in Fig. 1 extrapolated to $T \longrightarrow \infty$ provide $A_1 = 2.94 \times \exp [-1.02 \times 10^7/E]$ when $A_1$ is in $A/cm^2$ and E in V/cm where $A_1$ is the coefficient of the Frenkel-Poole relation

$$J_1 = A_1 \exp.[(-\frac{q}{kT})(\phi - B\sqrt{E_N})] \qquad (3)$$

The strong field-dependence of the pre-exponential factor $A_1$

invalidates determination of $\beta$ from measurements of steady state current vs. field at a fixed temperature by using $\beta = (kT/q)\, \partial \ell n\, J_{ST}/\partial \sqrt{E}$ .

The temperature - independent current levels $J_2$ are fitted by the Fowler - Nordheim relation[3]

$$J_2 = A_2 E_N \exp(-B/E_N) \qquad (4)$$

with $B = 2.07 \times 10^7$ cm/V and $A_2 = 6.18 \times 10^{-7}\ AV^{-1}cm^{-1}$.

In another set of experiments the flat-band voltage was first shifted toward its highest value by applying a large positive gate voltage and the initial charge build-up in the sample, by a sequence of negative gate pulses superimposed on flat-band, was then investigated. Figure 3 shows that the initial charge build-up in the nitride as registered by the charge amplifier in the MNOS circuit is well fitted by

$$Q = APq\ [\,1 - \exp(-t/t_T)\,] \qquad (5)$$

with $P = 10^{12}\ cm^{-2}$ and $t_T = 0.43$ms. Preliminary measurements at other temperatures and oxide fields show P and $t_T$ to be independent of temperature, P to be independent of

and $t_T$ to decrease strongly with oxide field.

The most interesting aspect of our data is the thermal activation of the current at elevated temperatures. While some temperature-dependence of the tunnel current may arise by tunneling of thermally activated carriers from the silicon, as proposed by Svensson and Lundstrom[4], we believe that this effect is too small to account for our observations. Rather than assuming tunneling into almost empty traps[4], we consider the occupancy of the traps into which the holes tunnel as the rate determining factor. This occupancy is determined by a dynamic equilibrium between the tunneling into the empty traps and emission from the filled traps. This emission occurs by the temperature dependent Frenkel-Poole mechanism at elevated temperatures, and trap occupancy and thus the tunnel current through the oxide then also becomes temperature-dependent.

We shall now describe a simple model which accounts for our experimental data. By lumping all hole traps which act as recipients for the oxide tunnel current into the $SiO_2/Si_3N_4$

interface, we have

$$\frac{dp}{dt} = \frac{P-p}{t_T} - \frac{p}{t_D} \qquad (6)$$

where P is the total number of hole traps per unit area, p is the number of occupied hole traps per unit area, $t_T$ is the time constant for a hole tunneling from the silicon into an empty hole trap and $t_D$ is the time constant for a hole leaving an occupied hole trap to enter the nitride valence band. The time constant $t_T$ is the reciprocal of the product of the arrival rate of holes at the oxide barrier, the probability to tunnel through it, and the capture cross section of an empty trap for a hole having tunneled through the barrier. The steady state current density is

$$J_{ST} = qp/t_D = qP/(t_D + t_T) \qquad (7)$$

Since we expect $t_T$ to be fairly independent of temperature, we conclude from the observed temperature dependence of $J_{ST}$ at elevated temperatures that $t_D >> t_T$ and that detrapping occurs by Frenkel-Poole emission. Since $t_D$ increases with

decreasing temperature while $t_T$ remains nearly constant, the same inequality should be even better satisfied at lower temperatures. The independence of temperature of the steady state current in the low temperature regime thus indicates that Fowler - Nordheim type tunnel emission of holes from the traps becomes dominant over Frenkel-Poole emission at the lower temperatures. Indeed the corresponding theoretical relations, equations (4) and (3), fit well the empirical steady state current data. The initial charge build-up of almost empty traps follows from Eqn. (6) for $p \ll P$ and gives Eqn. (5). The right uppermost experimental point in Fig. 3 falls above Eqn. (5) because detrapping can no more be neglected. The detrapping time constant for the data of Fig. 3 is $t_D \simeq qP/J_{ST} = 10$ m.sec which is large vs. $t_T$ in agreement with our model. The additional field $Pq/E_N \simeq 2.5 \times 10^5$ V/cm generated by the fully charged interface traps is still quite small vs. $E_{OX}\ \epsilon_N/\epsilon_{OX}$ which justifies neglecting the interface charge in the Frenkel-Poole plot of Fig. 2.

A more refined model which allows for spatial distribution for traps of a range of energy levels is now being investigated. The trap depth $\phi_T$ must then be considered an effective value which depends on temperature and field. This has implications for the interpretation of the parameters and A, derived from the experimental data. A volume trap distribution near the oxide-nitride interface has been invoked for the interpretation of charge retention data[5].

In conclusion, the temperature dependence of the steady state current through the oxide at elevated temperatures suggests that the tunneling of holes through the oxide is controlled by the availability of empty recipient states at, or close to the oxide-nitride interface. The degree of occupation of these interface hole traps is governed by a dynamic equilibrium between holes tunneling into these states from the silicon, and holes leaving the traps by a detrapping mechanism, which is of the Fowler - Nordheim type at low temperatures, and of the Frenkel-Poole type at elevated temepratures.

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Figure Captions.

Fig. 1. Temperature dependence of the steady state current through the dual dielectric of an MNOS capacitor measured at constant oxide fields pertaining to the pulse voltages indicated in Volts.

Fig. 2. A Frenkel-Poole plot of the activation energies derived from the slopes of the dashed lines in Fig. 1.

Fig. 3. Initial charge build-up in previously emptied interface traps when charging at constant oxide field corresponding to $V_p = -8V$ at room temperature.

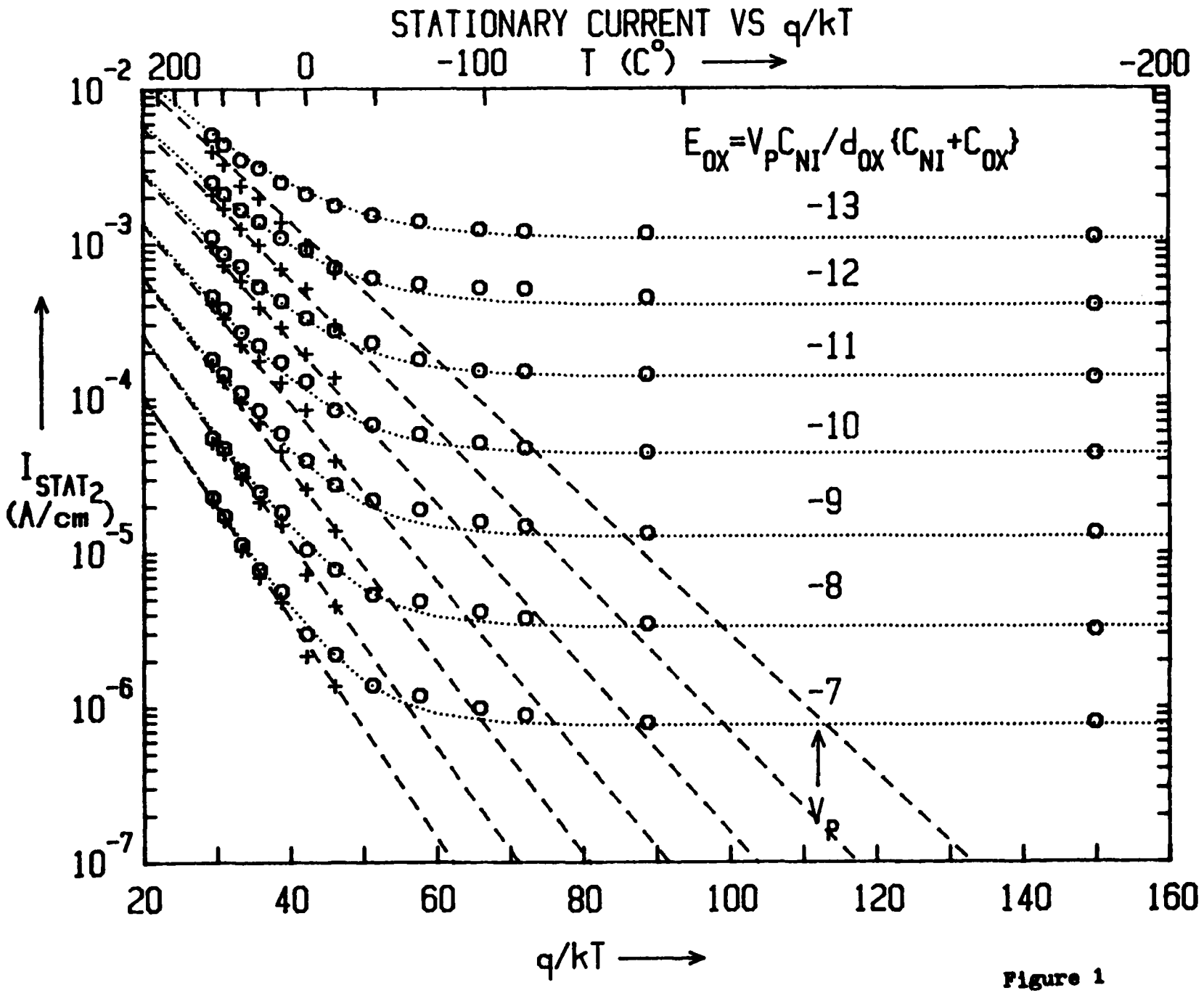
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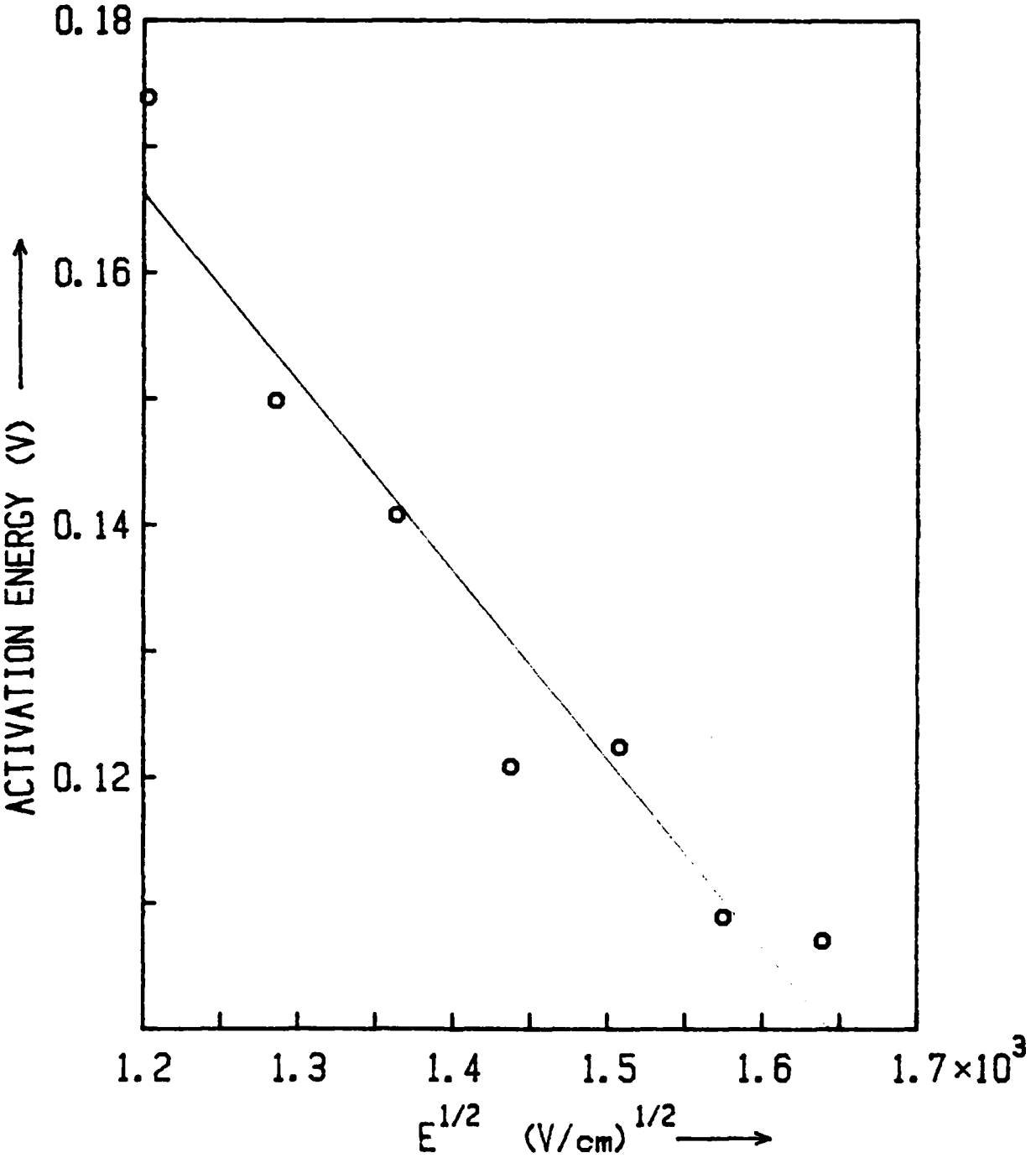
Figure 1

Figure 2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1.7×10^3
E^1/2 (V/cm)^1/2

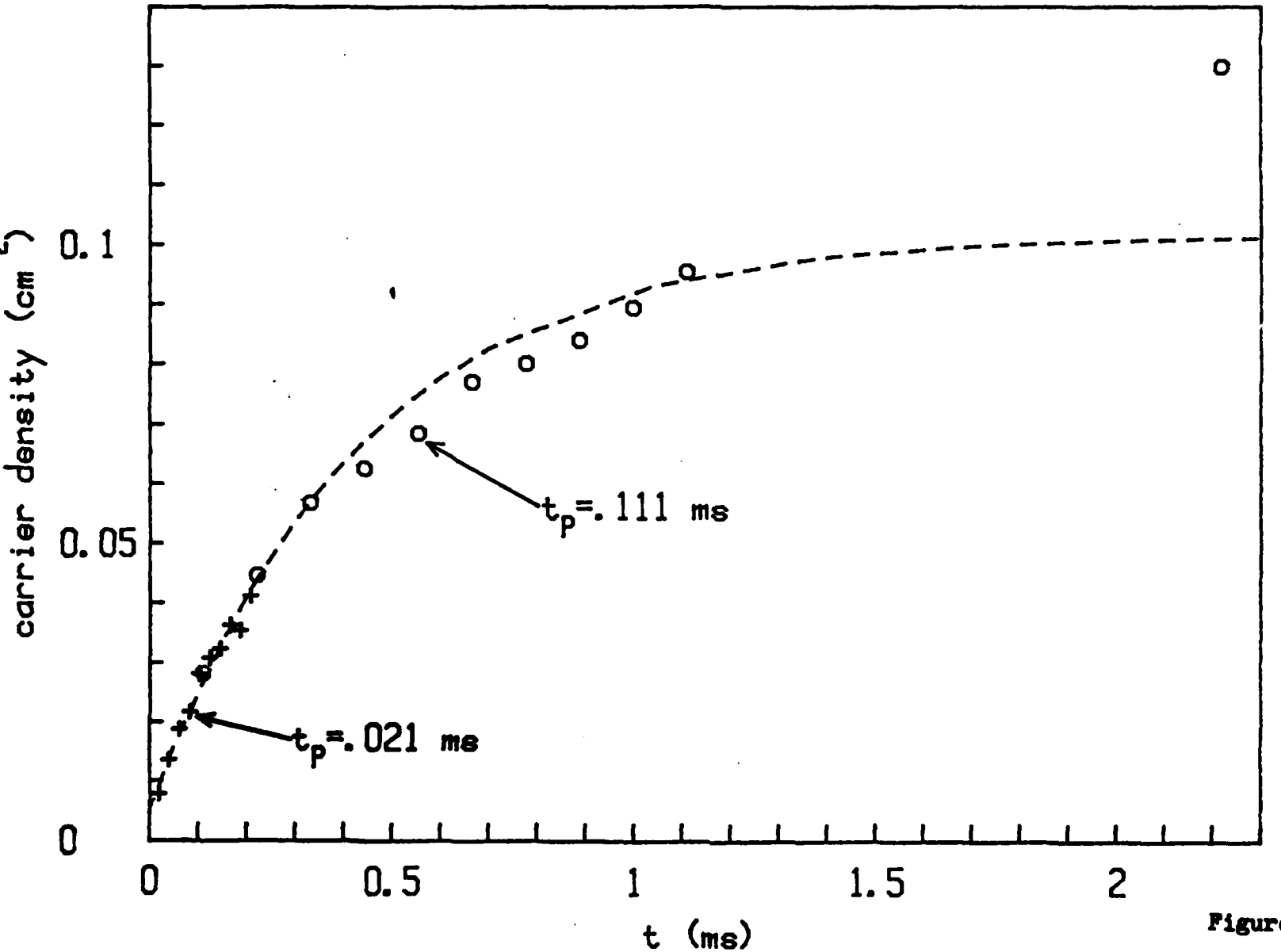


Figure 3

# Charge retention of MNOS devices limited by Frenkel-Poole detrapping[a)]

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A simple analytical expression is derived for charge retention in MNOS memory devices assuming that retention loss is limited by Frenkel-Poole release from monoenergetic traps. This model shows that charge retention becomes eventually independent of the initial charge distribution. Experimental data obtained at elevated temperatures confirm this model and provide a trap depth of 1.5 eV, Frenkel-Poole coefficient of about $6\times10^{-4}$ cm$^{1/2}$V$^{-1/2}$eV, and effective escape attempt rate factor of $1.2\times10^{6}$ sec$^{-1}$.

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Charge retention loss in thin oxide MNOS memory devices ($l_{ox} \lesssim 30$ Å) is dominated in its early stages by charge tunneling through the oxide from traps located at or near the oxide-nitride interface,[1–2] and in latter phases by Frenkel-Poole emission of charge trapped in the nitride and charge transport through the nitride.[3,4] In this paper we derive a simple analytic expression for the decay of retained charge based on Frenkel-Poole

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emission from monoenergetic traps. Following our procedure, an analytic expression can be derived for any other detrapping mechanism which depends solely on the local electric field intensity. The effect of retrapping can be accounted for by modifying the effective escape attempt factor.

After a charging pulse, the trapped nitride charge induces a charge of opposite polarity in the silicon and at the gate electrode (Fig. 1). This charge is not necessarily located at the silicon surface, as has been indicated, and there can be a potential drop, not shown in Fig. 1, across the silicon space-charge region. Ramifications of the charge distribution in the silicon and of the corresponding potential drop are discussed later in this paper. The potential distribution in the nitride has a minimum at a distance $x_m$ from the oxide.[4,5] This minimum is located closer to the oxide than to the gate, i.e., $x_m < \frac{1}{2}t_N$, since the concentration of trapped charge decreases with increasing distance from the oxide.[4,6-8] Consequently, the maximum nitride field during retention is located at the oxide interface. Thus detrapping occurs mostly near the oxide interface and the detrapped nitride charge shifts primarily toward the silicon. Therefore, the time dependence of the initial Frenkel-Poole-type detrapping in the region $0 \leq x \leq x_m$ provides a lower limit for charge retention.

The escape rate from traps will be assumed to obey the Frenkel-Poole law

$$\frac{\partial n_t}{\partial t} = -n_t \nu \exp[-\phi + \hat{\beta}(E)^{1/2}], \tag{1}$$

where $n_t(x,t)$ is the local trapped charge density and $E(x,t)$ is the local field, both functions of time. The notation here is the same as that used in Refs. 4, 7, and 8. Trapped charge density and field are related by Poisson's law

$$\frac{\partial E}{\partial x} = \frac{n_t q}{\epsilon_N}. \tag{2}$$

Thus

$$q\frac{d}{dt}\int_0^{x_m} n_t\,dx = -\nu\exp(-\hat{\phi})\epsilon_N\int_0^{E_0}\exp[\hat{\beta}(E)^{1/2}]dE + n_t(x_m)\,q\frac{dx_m}{dt} \tag{3}$$

with

$$E_0(t) = (q/\epsilon_N)\int_0^{x_m} n_t\,dx \tag{4}$$

FIG. 1. A typical charge and potential distribution during retention. The potential drop across the silicon space-charge layer is not shown, but is considered later in the text.

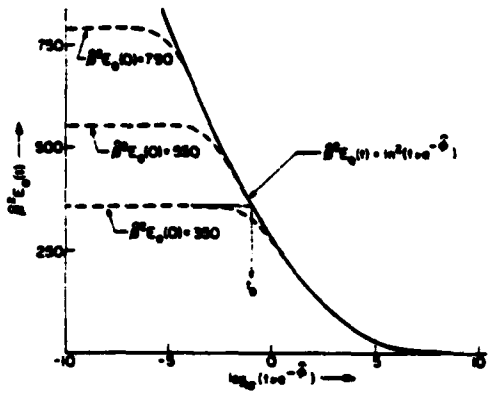


FIG. 2. The function $\hat{\beta}^2E_0(t)$ of $\nu t\exp(-\hat{\phi})$ according to Eq. (5) for different values of $\hat{\beta}^2E_0(0)$. In the range $\hat{\beta}[E_0(t)]^{1/2} \lesssim 1$, terms neglected in deriving Eq. (5) have been included in Fig. 2. to obtain $E_0(t) \to 0$ for $t \to \infty$.

the field in the nitride at the nitride/oxide interface, $x = 0$.

The second term on the right-hand side arises from the exchange of differentiation with respect to time, and of integration with respect to position, when proceeding from Eq. (1) to Eq. (3). For a constant potential applied between gate and silicon, the charge shift $qn_t(x_m)\,dx_m/dt$ can be related to the term on the left-hand side of Eq. (3), and to factors which involve the centroids of $q\int_0^{x_m}\partial n_t/\partial t\,dx$ and of the induced charge in the silicon. The latter is $\epsilon_s/C_{ss}$, where $C_{ss}$ is the low-frequency silicon space-charge capacitance. It can be shown that the right-hand side of Eq. (3) can be replaced by omitting the second term and multiplying the first term on that side by a factor $\eta$. This factor is significantly less than unity only in the depletion regime without inversion, and then only if $\epsilon_s/t_N C_{ss} \gtrsim 1$. The overall effect of this "$\eta$ dip" is always small, however, since at high dopant concentrations the dip is shallow, while at low dopant concentrations the dip is narrow because the $E_0$-field range pertaining to depletion without inversion becomes very small. We shall, therefore, neglect the last term of Eq. (3) in what follows.

Integration of the thus simplified Eq. (3), considering Eq. (4), provides

$$\hat{\beta}[E_0(t)]^{1/2} = \hat{\beta}[E_0(0)]^{1/2} - \ln[1 + \nu t\exp(-\hat{\phi}) \times \exp[\hat{\beta}(E_0)^{1/2}]], \tag{5}$$

where certain terms have been neglected for convenience, assuming that $\hat{\beta}[E_0(t)]^{1/2} \gg 1$. The function $\hat{\beta}^2E_0(t)$ versus $\log[\nu t\exp(-\hat{\phi})]$ is shown in Fig. 2 for various values of $\hat{\beta}^2E_0(0)$ chosen to provide $t_0 = \nu^{-1}\exp\{\hat{\phi} - \hat{\beta} \times [E_0(0)]^{1/2}\}$ of $10^{-1}$, $10^{-3}$, and $10^{-6}$ sec, respectively. All curves merge into the same unique function

$$\hat{\beta}^2E_0(t) = \ln^2[\nu t\exp(-\hat{\phi})] \tag{6}$$

for

$$t_0 \ll t \ll \nu^{-1}\exp(+\hat{\phi}). \tag{7}$$

The field intensity $E_0(t)$ in the nitride at the boundary of the oxide can be related to the threshold voltage by the following considerations. The threshold voltage with nitride charge differs from that without nitride charge

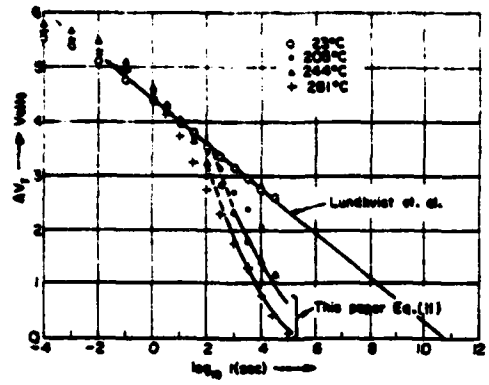


FIG. 3. Experimental charge retention loss fitted by Eq. (11).

(so-called "intrinsic state") by

$$V_T(t) - V_T(\infty) = \left(\frac{q}{\epsilon_N}\right)\int_0^{t_N} n_t(t_N - x)\,dx$$

$$= \left(\frac{qt_N}{\epsilon_N}\right)\int_0^{x_m} n_t\,dx - \frac{q}{\epsilon_N}\int_0^{x_m} n_t x\,dx$$

$$+ \left(\frac{q}{\epsilon_N}\right)\int_{x_m}^{x_N} n_t(t_N - x)\,dx. \qquad (8)$$

The first of the last three terms is $E_0(t)\,t_N$; the second term is the potential drop between $x = 0$ and $x_m$; and the third term is the potential drop between $x_m$ and $t_N$. In a typical retention experiment a constant bias voltage $V_A$ is applied between gate electrode and silicon substrate. Since

$$V_A + V_B = V_{sp} - \left(\frac{\epsilon_N}{\epsilon_0}\right) t_{ox} E_0 - \left(\frac{q}{\epsilon_N}\right)\int_0^{x_m} n_t x\,dx$$

$$+ \left(\frac{q}{\epsilon_N}\right)\int_{x_m}^{t_N} n_t(t_N - x)\,dx, \qquad (9)$$

where $V_{sp}$ is the potential across the space-charge layer in the silicon and $V_B$ is the built-in potential between gate and substrate, Eq. (8) can be transformed into

$$V_T(t) - V_T(\infty) = E_0(t)[t_N + \epsilon_N t_{ox}/\epsilon_{ox}] + V_A + V_B - V_{sp}. \qquad (10)$$

The built-in potential compensates closely the space-charge layer potential in case of a $p^+$-polysilicon gate and an $n$-type substrate if the nitride charge induces an inversion layer in the silicon. Under this condition, one obtains from Eqs. (10) and (6) for retention at zero gate to substrate bias voltage

$$V_T(t) - V_T(\infty) \cong t_N \hat{\beta}^{-2} \ln^2[\nu t \exp(-\hat{\phi})]. \qquad (11)$$

This equation is valid for $t \gg t_0$.

Figure 3 shows experimental data supplied by Dr. M. Beguwala of Rockwell International. The nitride was charged by applying positive voltage pulse to the gate of an MNOS capacitor on $n$-type silicon substrate at various temperatures indicated in Fig. 3. The device was at its intrinsic threshold voltage prior to pulsing. The lack of a significant temperature dependence for $t \lesssim 100$ msec suggests that retention loss is initially governed by tunneling. The straight line in Fig. 2 is the tunnel relation of Ref. 1. After about 1 sec detrapping appears to become the dominant factor for retention loss at the elevated temperatures. The retention period when initial charge distribution has an effect on the detrapping rate is masked by tunnel escape. The drop-off of the data points at 281 °C was fitted by Eq. (11) with $\beta = \hat{\beta}kT/q = 5.2\times10^{-4}$ cm$^{1/2}$V$^{-1/2}$eV, $\phi = 1.5$ eV, and $\nu = 1.2\times10^{5}$ sec$^{-1}$ determined as follows: A plot of $\ln V_T$ versus $\log_{10}t$ of the experimental values was matched to a plot of $\ln E_0$ versus $\log_{10}[\nu\exp(-\hat{\phi})t]$ according to Eq. (11); the displacement along the ordinate is $\ln(t_N\hat{\beta}^{-2})$ and the displacement along the $x$ axis is $\log_{10}[\nu\exp(-\hat{\phi})]$. The parameters $\nu$ and $\phi$ have been separated by applying the same procedure to the data at 244 °C and assuming that $\nu$ is independent of temperature. The $\beta$ value pertaining to 244 °C was $6.4\times10^{-4}$ cm$^{1/2}$V$^{-1/2}$eV. The slight temperature dependence of $\beta$ should be confirmed by additional experimental data before attempting an interpretation. The $\beta$ values are about twice the accepted value for the Frenkel-Poole coefficient.[7,9–12] The comparatively small value of $\nu$ may be indicative of a positive temperature coefficient of the trap depths, $d\phi/dT > 0$, and of retrapping. The time $t$ used in the theoretical expression (11) is the initial detrapping time, $t_{th} = \tau_t$. On the other hand, the time of the experimental points is the time when trapped electrons are removed from the nitride, i.e., $t_{exp} = \tau_t + \theta$. These times differ by the delay $\theta$ due to retrapping.

Since, by curve fitting, $\nu_{th}t_{th} = \nu_{exp}t_{exp}$ we have

$$\nu_{exp} = \frac{\nu_{th}}{1 + \theta/\tau_t} = \nu^* \exp\left[-\left(\frac{d\phi}{kdT}\right)\left(1 + \frac{\theta}{\tau_t}\right)\right]^{-1}, \qquad (12)$$

where $\nu^*$ is the intrinsic escape attempt frequency, usually assumed to be of the order of the vibrational lattice frequency. The delay time $\theta$ is expected to be a weak function of time, and this implicit time dependence should not affect Eq. (11) strongly.

The observed temperature dependence in the temperature range 154–205 °C was less than that expected by our theory, with $\phi$ and $\nu$ as derived from the data obtained at 244 and 281 °C. This discrepancy is attributed to a second, more shallow, trap level which becomes dominant (filled) at the lower temperatures and which is *insignificant* (empty) at the more elevated temperatures. Unfortunately, Eq. (3) written for the case of multiple trap levels cannot be integrated to provide a concise form such as Eq. (5) for the retention loss arising from the detrapping of electrons from a single trap level.

Our model provides a concise analytical expression for the charge retention loss if all traps have the same activation energy. During the latter periods of retention loss, this expression becomes independent of the initial charge distribution, and depends then only on trap depth, Frenkel-Poole coefficient, and an effective escape attempt rate factor which takes into account retrapping.

We thank Dr. M. Beguwala and Dr. Ross Williams of Rockwell International for supplying the experimental data and for helpful discussions.

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# MNOS Charge Versus Centroid Determination by Staircase Charging

KURT LEHOVEC, FELLOW, IEEE, CHIH-HONG CHEN, AND ANDRE FEDOTOWSKY

*Abstract*—The charge versus centroid relationship is determined by staircase charging, in which a sequence of identical pulses is applied, the memory device is returned to flat-band condition after each pulse, and the subsequent pulse is superimposed on the flat-band voltage corresponding to the accumulated memory charge distribution resulting from the preceding pulses. Staircase patterns of accumulated negative charge and of device voltage are analyzed, and effects arising from back-tunneling and leakage currents are identified. Comparison of the initial injection current during a voltage pulse with the steady-state current indicates that hole injection from the gate does not contribute significantly to the steady-state oxide tunnel current.

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## I. INTRODUCTION

ARNETT AND YUN [1], [2] have determined the memory charge versus centroid relationship for electron injection from the silicon by using a sequence of large-voltage pulses of increasing duration to charge the nitride of MNOS devices [Fig. 1(a)]. The Yun method restores the sample to its initial charge-free state before the next charging pulse is applied. The memory charge is removed by applying pulses of opposite polarity and of appropriate magnitude and duration until the flat-band voltage reaches a predetermined value believed to be characteristic of the memory charge free state. Restoration of this flat-band voltage after each voltage pulse is time consuming, since it must be achieved by trial and error. Moreover, reverse polarity pulsing may not only remove negative charge injected by preceding pulses, but also inject positive charge into the nitride. Since certain superpositions of positive and negative charge distributions give rise to a flat-band voltage

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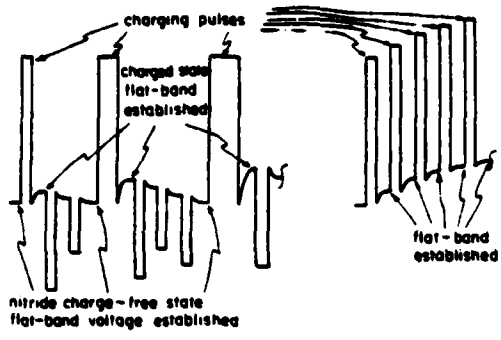


Fig. 1. Voltage profiles for charge versus centroid determination. (a) Yun method [1], in which the sample is returned to flat band following each charging pulse application and then brought to the charge-free state by reverse polarity pulsing before the next charging pulse of increased duration is applied. (b) Staircase-charging method, in which the sample is also returned to flat band, but the charge is allowed to accumulate step-wise by application of a train of identical charging pulses.

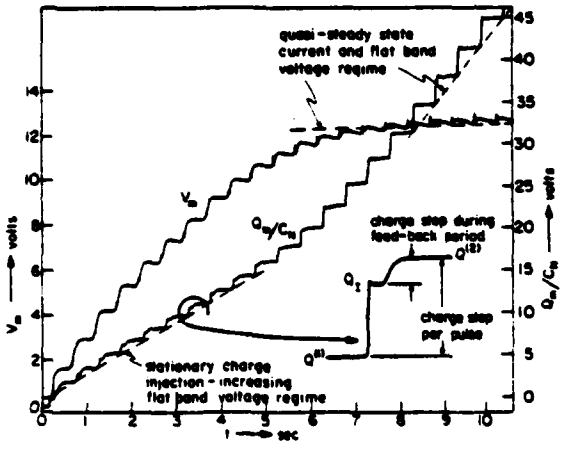


Fig. 2. A typical voltage and charge profile for the staircase charging method obtained by positive voltage pulses applied to the gate electrode. n-type silicon substrate of 1.4-Ω · cm resistivity; $t_{ox}$ = 22 Å; $t_N$ = 285 Å; $V_p$ = 10 V; $t_p$ = 1 ms; $t_R$ = 0.5 s.

equal to that of the charge-free state, generating this flat-band voltage by reverse polarity pulsing does not guarantee achievement of the charge-free state.

We describe in this paper a technique by which a sequence of small identical voltage pulses is applied to the device to increase the nitride memory charge in a staircase pattern [Fig. 1(b)]. Flat-band condition is restored between these pulses by a feedback circuit, as in the Yun method, but unlike the Yun method, the initial charge-free state is not re-established. The staircase patterns shown in Fig. 2 are recordings of the charge $Q_m$ which has passed through the external circuit to the gate, and of the flat-band voltage $V_m$ across the sample. These recordings were obtained in less than a minute and contain all the information required for a complete charge versus centroid determination. We provide the derivation of the charge versus centroid relation from the staircase patterns, and we show that the data acquired by the staircase charging method yield information about other important MNOS device properties, such as memory retention loss and charging current as a function of the applied voltage.

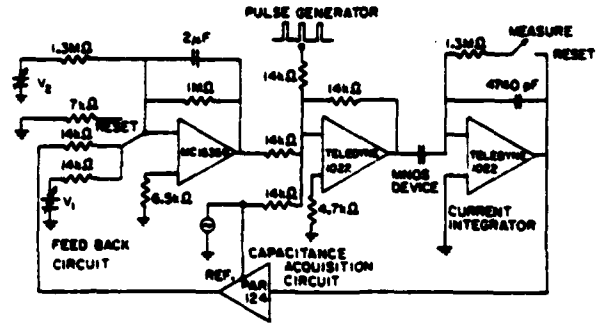


Fig. 3. Block circuit diagram for applying the voltage pulses, sensing deviation from flat band by capacitance measurements, returning the sample to flat band by a feedback circuit, and measuring the charge passed through the silicon–oxide interface by a current integrator.

## II. Measurement Technique

The measuring circuit (Fig. 3) is essentially that of [3]. A small ac voltage is applied to the MNOS capacitor; the capacitance is measured by a lock-in amplifier circuit and compared to a fixed reference capacitance equal to the flat-band capacitance. The difference between the measured MNOS capacitance and the reference capacitance generates a dc bias voltage in a feedback circuit which returns the device to flat band after each voltage pulse. The time interval $t_{FB}$ for restoration of flat band (feedback period) includes the acquisition time for capacitance sensing by the lock-in amplifier, and several cycles of bias voltage readjustment until the measured capacitance equals the flat-band capacitance. The feedback period must be long compared to the pulse duration $t_p$ to prevent automatic bias voltage adjustment during the pulse by the feedback circuit. On the other hand, if the feedback period is too long, charge retention loss between pulses increases, and the charge measured by the current integrator differs increasingly from the nitride charge, due to device leakage currents of presently unknown origin shunting the MNOS dielectric. For the same reasons the "rest period" $t_R$ between pulses should not be much longer than $t_{FB}$. A typical set of time constants as used in our experiments is given in Table I. The measured voltage $V_m$ equals the flat-band voltage $V_{FB}$ during the time interval $t_R - t_{FB}$.

Consider a nitride charge-free sample at flat-band voltage $V_{FB}^{(1)}$ at time $t_1$. The sample then acquires a negative nitride charge $-Q$ by application of a positive voltage pulse(s) and is at the flat-band voltage $V_{FB}^{(2)}$ at time $t_2$. Since the charge in the silicon has not changed, the entire charge

$$Q_m = \int_{t_1}^{t_2} I\,dt \tag{1}$$

flowing through the external circuit to the gate during the intermediate period $t_1 < t < t_2$ has crossed the silicon-silicon oxide interface. Thus $Q_m$ equals the absolute value $Q$ of the nitride charge provided that: 1) no injected charge has left the sample at the gate; 2) no positive charge injection from the gate has taken place; and 3) the charges in surface states and in the oxide have not changed. If the sample is charge free at $t_1$ and has acquired the negative charge $-Q$ at $t_2$, the centroid of $-Q$ is

TABLE I
TYPICAL TIME CONSTANTS PERTAINING TO THE CIRCUIT OF FIG. 3

| | |
|---|---|
| a.c. Signal (10 kHz) | 1/f = 0.1 ms |
| Lock-in acquisition time | 1 ms |
| Feed back circuit time constant | 50 ms - 200 ms |
| Pulse duration | 5 microsecond - 10 ms |

$$\bar{x} = t_N [1 - C_N(V_{FB}^{(2)} - V_{FB}^{(1)})/Q] \quad (2)$$

with $V_{FB}^{(2)}$ and $V_{FB}^{(1)}$ the flat-band voltages at $t_2$ and $t_1$, $t_N$ the nitride thickness, and $C_N$ the nitride capacitance. Thus the staircase charging technique can be used to derive the charge versus centroid relation provided that we include in (1) and (2) the total charge injected by all previous pulses, and that we use the total flat-band voltage change from the initial charge-free state. Charge corrections required to account for parasitic charge added by a shunt leakage path to, or in, the MNOS dielectric are discussed in Appendix I.

Replacing the total nitride charge $Q = Q^{(1)} + \delta Q$ on the right-hand side of (2) by the charge $\delta Q = Q^{(2)} - Q^{(1)}$ added to the nitride by the voltage pulse, we obtain

$$x^* = (\delta Q x_\delta + Q^{(1)}\delta x_1)/\delta Q = t_N [1 - C_N(V_{FB}^{(2)} - V_{FB}^{(1)})/\delta Q]. \quad (3)$$

The length $x^*$ represents the centroid of the difference between the nitride charge distributions pertaining to $Q^{(1)}$ and $Q^{(2)} = Q^{(1)} + \delta Q$. We are not aware of any method which might distinguish between the contribution to $x^*$ from the centroid $x_\delta$ of the charge $-\delta Q$ added to the nitride and that of the shift $\delta x_1$ of the centroid $x_1$ of the charge $-Q^{(1)}$ present in the nitride prior to application of the pulse. However, measured data of $x^*$ could be compared with theoretical values derived from models for the nitride charge distribution based on "negligible detrapping" [2], "strong detrapping" [4], [5], and "nitride charge loss by back-tunneling" [6] during the feedback period.

## III. INTERPRETATION OF STAIRCASE CHARGING PATTERNS

The staircase charging method provides capability for investigating charge buildup, or removal, by positive or negative gate pulses. Negative gate voltage pulses initially cause deep depletion of the silicon surface which may reduce the oxide and nitride fields significantly until an inversion charge has built up. This buildup can be accelerated by illumination with light of suitable wavelength. Nevertheless, we shall present here only the results of investigations related to positive gate pulses applied to n-silicon devices in order to avoid complications of interpretation associated with deep depletion by negative voltage pulses. The positive pulse voltage causes accumulation of the silicon surface and thus extends across the oxide and nitride layers.

The inset in Fig. 2 shows that the charge change caused by a voltage pulse is composed of a first step to an intermediate charge level $Q_I$, followed by a second step to the final charge level $Q^{(2)}$. It is shown in Appendix II that the intermediate charge level can be expressed in terms of the initial and final charge levels, the change in the flat-band voltage, and the $C$-$V$ relation. Thus measurement of $Q_I$ is superfluous for investigating the nitride charge and its distribution.

The charge registered by the current integrator may decrease during the early part of the feedback period, as shown in the inset of Fig. 2. This is attributed to memory charge loss by back-tunneling [3], [6]. The charge indicated by the current integrator after flat band has been achieved is the injected charge less the back-tunneled charge, i.e., the remaining charge in the nitride, and its centroid is given by (2).

The charge and voltage staircase patterns recorded in Fig. 2 exhibit the following interesting features:

*1) Charge Staircase Pattern:* The charge step per pulse first decreases slightly, then remains stationary for a number of pulses, and then increases to a steady-state value. The portion of charge added during the feedback period *after* each pulse decreases with the number of pulses and almost vanishes when the steady state is reached.

*2) Voltage Staircase Pattern:* The flat-band voltage change per pulse decreases with the number of pulses until a steady-state average level is reached. The voltage increase during $t_{FB}$ is then compensated by a flat-band voltage decrease during $t_R$-$t_{FB}$. The decay of flat-band voltage during the rest period is noticeable only after several pulses have been applied, becoming most pronounced when the steady-state level has been reached.

These observations have the following explanations. The charge injected per pulse into the nitride decreases initially because receptor states located either in the oxide or at the oxide-nitride interface become saturated. The excess charge of the first charge step amounts to $7.5 \times 10^{+11}$ cm$^{-2}$ states for the sample of Fig. 2. The several subsequent charge steps are very nearly equal. This behavior is expected because charge tunneling through the oxide is controlled by the oxide field which is the same at the beginning of each pulse since each pulse is applied at flat-band bias. The decrease in the corresponding flat-band voltage change per pulse with the number of pulses indicates that the centroid of charge moves more deeply into the nitride with each successive pulse. This shift of the centroid arises from detrapping and deeper penetration of charge injected by previous pulsing [4], [7]. Newly injected charge may also penetrate further because some of the traps may have been filled by previously injected charge [2].

Subsequent to this "stationary charge injection-increasing flat-band voltage regime" (Fig. 1), the charge per pulse increases until it reaches a steady-state value. This has the following explanation: Fig. 4 illustrates the time dependence of charge injected through the oxide into the nitride during a sequence of pulses. Each pulse is imposed on flat-band voltage, so that the initial oxide field, and thus the initial injection current, remains constant for all pulses. The injected charge reduces the oxide field, and thus the injection current decreases during each pulse. The added space charge during each pulse diminishes as charge injection through the oxide is partially compensated by charge exit from the nitride into the gate electrode. The steady state reached after many pulses indicates that most of the charge now passes through the entire nitride, i.e., as much charge leaves through the gate as is added through

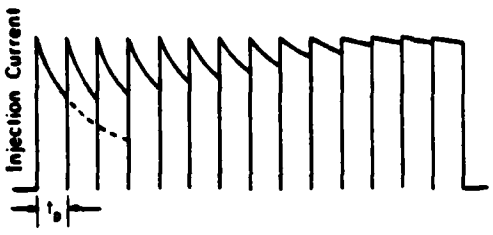


Fig. 4. Injection currents for a voltage pulse train with flat band re-established between pulses; rest period $t_r$ between the pulses not shown. The current decays during each pulse because the injected charge reduces the oxide field. This reduction diminishes with increasing number of pulses, as charge injection is increasingly compensated by charge exit from the nitride into the gate.

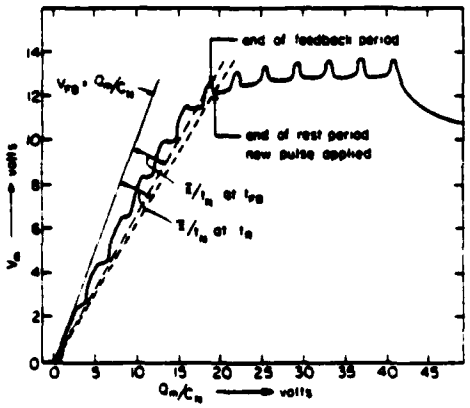


Fig. 5. Recording of device voltage versus accumulated charge using $V_p = 15$ V, $t_p = 10$ μs, and $t_r = 0.5$ s. The deviation of the slopes of the straight dotted lines from the reference line $V_{FB} = Q_m/C_N$ of slope 1 provides $\bar{x}/t_N$ in the absence of leakage charge accumulation.

the oxide (or vice versa for positive charges injected from the gate). Only a small nitride charge is added by each pulse to compensate for the retention charge loss during the preceding feedback and rest periods. This added nitride charge, and the retention charge loss by back-tunneling to the silicon [3], [6], account for the voltage pattern during the feedback and rest periods in the steady state. The fact that the flat-band voltage does not visibly decay after the early pulses, but does decay after many pulses, is attributed to increased back-tunneling which results from charge buildup in the nitride at the oxide interface [4], [7].

Fig. 5 is an *X-Y* recording of the device bias voltage as a function of the accumulated charge in the current integrator. The maxima in the quasi-steady-state regime occur at the end of the feedback periods. During the subsequent rest periods, the flat-band voltage decays due to back-tunneling. However, the charge increases because leakage current exceeds the back-tunnel current. The abrupt transition from a decline to a horizontal indicates that a voltage pulse has been applied. The horizontal region results from charge flow during the pulse. The subsequent maximum arises from the charge and voltage increases during the feedback period. Maxima associated with early pulses are not discernible because the nitride charge has not yet accumulated to the extent required for pronounced back-tunneling. Hence, the leakage charge accumulated during the rest period prior to the start of an early

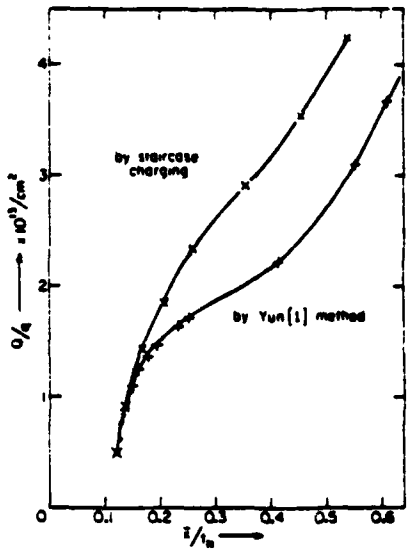


Fig. 6. Charge versus centroid curves for electron injection from the silicon derived by the staircase-charging technique using $V_p = 16$ V, $t_p = 10^{-6}$ s, and $t_r = 0.5$ s; and by the single-pulse method [2] using $V_p = 16$ V(·), and $V_p = 20$ V (+).

pulse is indistinguishable from the nitride charge injected during the pulse period. In absence of a leakage charge, the slope of a line connecting the origin to a point pertaining to flat band is $1 - x/t_n$, according to (2).

## IV. Experimental Charge Versus Centroid and Injection Current Polarization Data

Fig. 6 compares a charge versus centroid curve obtained by the Yun method with that derived by the staircase charging method. The first pulse is the same in both methods, and the data point pertaining to the extrapolated intercept $\bar{x}(Q \to 0)$ which gives the range of the electrons injected into the charge-free nitride is about the same for both methods.

The difference between the charge versus centroid relations obtained by the Yun method and by the staircase method at higher charge levels depends on pulse voltage and duration, and on the rest period between pulses. We attribute this difference to different charge distributions arising mainly from different injection current versus time relationships for the two methods. The dotted line in Fig. 4 shows that the injection current during a single pulse of duration $3t_p$ changes more than the injection current during three successive identical voltage pulses of the staircase method each of duration $t_p$. Thus the staircase charging technique approaches constant current pulse conditions more closely than does the Yun technique, which uses constant voltage pulses of increasing duration. Charge versus centroid curves for constant voltage pulse are expected to differ from those for constant current pulses [5]. Moreover, the theoretical analysis of charge versus centroid data obtained by constant current pulses is simpler than that obtained by constant voltage pulses [5].

Back-tunneling of nitride charge to the silicon during the rest period between pulses of the staircase charging method temporarily reduces the nitride charge near the oxide boundary. This charge is replenished immediately by the pulse following

the rest period. The charge integrator registers the net charge which crosses the oxide–nitride interface. Thus the contributions from the back-tunnel charges and their replenishment cancel. Nevertheless, after several pulse applications, the charge centroid differs somewhat from that which would have been obtained with a single long pulse, during which back-tunnelling and back-tunnelling replenishment do not occur.

Charge step per pulse in the quasi-steady-state regime, marked in Fig. 2, divided by the pulse duration, provides the steady-state oxide current at a gate voltage equal to the sum of flat-band bias voltage and pulse voltage. In the case of Fig. 2, this voltage sum is 22.5 V. Holes injected from the gate, crossing the entire nitride, and entering the silicon through the oxide, would contribute to this current. On the other hand, holes injected from the gate and recombining with electrons before entering the silicon through the oxide, do not contribute to this current, since the charge $Q_m$ registered by the current integrator is the charge passing through the oxide. A hole injected from the gate partway into the nitride contributes to the charge registered by the charge integrator during the voltage pulse. However, this contribution is compensated exactly when flat-band voltage is subsequently re-established during the feedback period. Holes injected from the gate cannot reach the oxide interface during the first several pulses of combined duration less than the transit time of the holes through the nitride. Thus the initial oxide current during these early pulses arises only by electron injection from the silicon. The excess of the oxide current in the quasi-steady-state regime over the initial pulse current in the "stationary charge injection-increasing flat-band regime," marked in Fig. 2, provides, therefore, the current of holes injected from the gate and penetrating through the entire nitride film.

The initial pulse current during the "stationary charge injection-increasing flat-band voltage regime" has been determined from a series of staircase patterns pertaining to different pulse durations $t_p^{(n)}$ by the procedure indicated in Fig. 7. The theoretically expected time constant for the injection current decay is

$$-\frac{\partial t}{\partial \ln I} = -\frac{\partial t}{\partial E_{ox}} \, 2\sqrt{E_{ox}} \, \frac{\partial \sqrt{E_{ox}}}{\partial \ln I}$$

$$= \frac{2A}{I} \epsilon_{ox} \sqrt{E_{ox}} \, \frac{\partial \sqrt{E_{ox}}}{\partial \ln I}. \quad (4)$$

The factor $\partial\sqrt{E_{ox}}/\partial \ln I$ calculated for oxide tunneling by electrons is 130 $cm^{1/2} \cdot V^{-1/2}$ for an oxide thickness of about 20 Å and an oxide field of about $10^7$ V/cm according to [5, fig. 1]. The decay of the injection current is not exponential, since the time constant depends on the current. Using the $e^{-1}$-th value of the initial current density of Fig. 7 we obtain by (4) a time constant of about $10^{-5}$ s, in good agreement with the observed current decay.

The pulse current of Fig. 7 extrapolated to very short pulse duration is found to equal within ± 20 percent the steady-state nitride current. We conclude that in the sample of Fig. 7 at the applied voltage injected holes, if any, recombine with electrons before reaching the oxide [8], provided that the hole transit time is longer than about 5 μs. Hole injection from the gate would have little effect on the flat-band voltage initially,

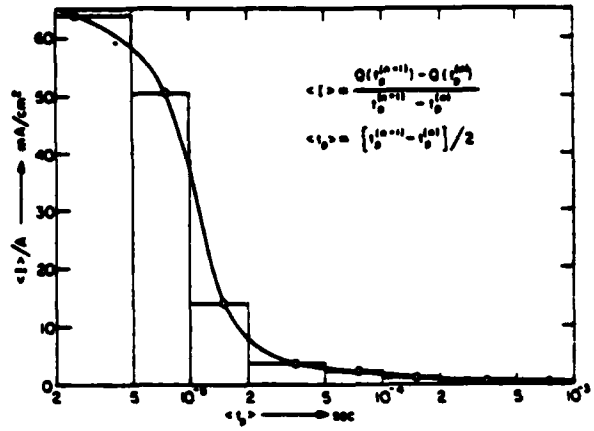


Fig. 7. Injection current versus time profile derived from the "stationary charge injection-increasing flat-band voltage regime" (Fig. 2) for a set of staircase-charging experiments with identical pulse height of 15 V and pulse durations ranging from 5 μs to 1 ms. The index $n$ distinguishes pulse trains of different pulse durations.

since nitride charge contributes to the flat-band voltage in proportion to its distance from the gate. Absence of a significant hole injection from the gate has been demonstrated also by [9]. However, our more recent experiments have shown a finite hole injection from the aluminum gate which depends less strongly on the pulse voltage than the electron injection from the silicon. Thus the fraction of the steady-state current carried by holes increases as the gate voltage decreases.

## V. Summary and Conclusions

The memory charge versus centroid relationship has been determined by a new, nondestructive technique in which a sequence of identical pulses is applied to the device, and the charge through the external circuit, and voltage across the device, are recorded as functions of time. The device is returned to flat band between pulses by means of a bias voltage applied to it from a feedback circuit. Each successive pulse is superimposed on the flat-band voltage corresponding to the accumulated memory charge distribution resulting from preceding pulses. Effects arising from back-tunneling and leakage currents during rest periods between pulses have been identified in representative charge and voltage "staircase" patterns obtained with this technique. Many data have been acquired by varying pulse height, rest period, and pulse duration. These data will be reported and analyzed in a subsequent paper.

The "staircase charging" method provides, in addition to the charge versus centroid relationship, the steady-state current for the fully charged memory device, the leakage current at various memory charge and flat-band voltage levels, and memory charge retention loss data. Staircase charging can be interrupted at any desired charge or flat-band voltage level, and the decay of flat-band voltage and charge changes can be registered as functions of time to indicate the back-tunneling of memory charge. A discharge staircase pattern can be used to study the emptying of memory charge by reverse polarity pulsing.

The principal advantage of our technique is the rapidity with which the raw data are obtained. When this method is applied to leaky devices, a correction for the leakage charge is required. Although we have provided a procedure for making this cor-

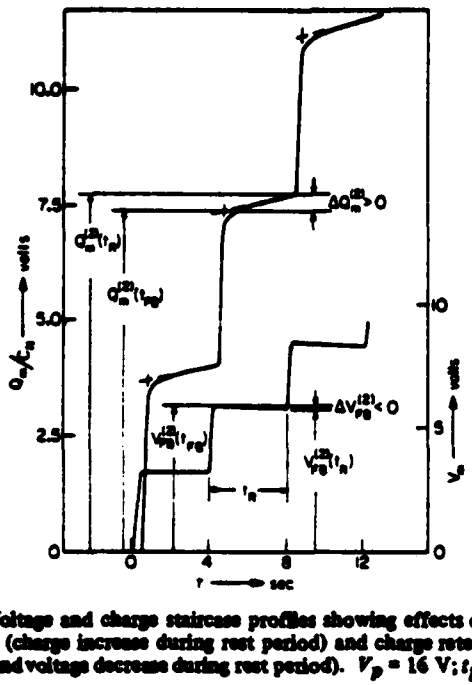


Fig. 8. Voltage and charge staircase profiles showing effects of leakage current (charge increase during rest period) and charge retention loss (flat-band voltage decrease during rest period). $V_p = 16$ V; $t_p = 10$ μs.

TABLE II
CENTROID $\bar{x}$ AND CHARGE $Q$

| Pulse Number | | at $t_{FB}$ | | at $t_R$ | |
|---|---|---|---|---|---|
| | | $\bar{x}/t_N$ | $Q/q$ ( $10^{11}$/cm$^2$) | $\bar{x}/t_N$ | $Q/q$ ( $10^{11}$/cm$^2$) |
| n = 1 | i | .139 | 91.3 | .212 | 98.9 |
| | ii | .139 | 91.3 | .142 | 91.3 |
| | iii | .139 | 91.3 | .139 | 91.1 |
| n = 2 | i | .203 | 102.3 | .249 | 106.9 |
| | ii | .161 | 97.1 | .186 | 97.1 |
| | iii | .156 | 96.9 | .163 | 95.8 |
| n = 3 | i | .241 | 155.2 | .287 | 161.3 |
| | ii | .190 | 145.4 | .209 | 145.4 |
| | iii | .182 | 144.0 | .194 | 142.7 |

i) From uncorrected data.
ii) Corrected for leakage current ignoring flat-band voltage decay.
iii) Corrected for leakage current and flat-band voltage decay.

rection, we are now developing a circuit modification which will suppress the leakage charge accumulation by reducing the rest period between pulses to the 10-ms range. This will be accomplished by replacing the feedback circuit with a PDP-11 Data Acquisition System programmed in machine language. The ultimate time limitation will then be governed by acquisition of the capacitance data in the lock-in amplifier circuit.

## Appendix I
## Corrections for Charge Versus Centroid Determination in Case of Charge Leakage

Fig. 8 shows a case for which flat-band voltage decreases and charge increases during the period $t_R$-$t_{FB}$. The rest period between pulses was chosen unusually long to accentuate the changes occurring after flat band has been achieved. The feedback period $t_{FB} = 50$ ms, after which flat band is established, is not discernable on the time scale shown. The subsequent change of flat-band voltage with time during the rest period is sufficiently slow that flat-band voltage is maintained by the feedback circuit.

Several corrections to the charge have to be made before evaluating charge versus centroid from these data by (1) and (2). These corrections are based on the assumptions that: 1) the slope of charge versus time during the rest period results, at least in part, from a leakage current which shunts the dielectric, and 2) the change in flat-band voltage during the rest period results from back-tunneling of negative charge $Q_T = C_N \Delta V_{FB}$ to the silicon. The nitride charge content $Q$ is decreased by the back-tunnel charge $Q_T$, and the observed $\Delta Q_m$ is thus the "leakage charge" minus the back-tunnel charge. The "leakage charge" $\Delta Q_m - Q_T$ is larger than $\Delta Q_m$.

In Table II we list values of charge $Q$ and centroid $\bar{x}$, obtained by (2), using $V_{FB}(t_R)$, with $Q(t_R)$ related to the measured $Q_m(t_R)$ as follows:

i) $Q(t_R) = Q_m(t_R)$

ii) $Q(t_R) = Q_m(t_R) - \sum_{1,n} \Delta Q_m^{(\nu)}$

iii) $Q(t_R) = Q_m(t_R) - \sum_{1,n} \Delta Q_m^{(\nu)} + C_N \sum_{1,n} \Delta V_{FB}^{(\nu)}$.

Similarly, we use $V_{FB}(t_{FB})$ and the following values for $Q(t_{FB})$:

i) $Q(t_{FB}) = Q_m(t_{FB})$

ii) $Q(t_{FB}) = Q_m(t_{FB}) - \sum_{1,n-1} \Delta Q_m^{(\nu)}$

iii) $Q(t_{FB}) = Q_m(t_{FB}) - \sum_{1,n-1} \Delta Q_m^{(\nu)} + C_N \sum_{1,n-1} \Delta V_{FB}^{(\nu)}$

for charge versus centroid determination at $t_{FB}$.

Table II shows that the correction for the back-tunnel charge (iii versus ii) is not significant. However, elimination of the leakage charge (ii versus i) is an important correction in case of Fig. 8.

## Appendix II
## Integrator Charge Versus Time During the Voltage Pulse and the Feedback Period

Application of the voltage pulse causes an immediate charging current spike. Its charge

$$Q_C = \int_{V_{FB}^{(1)}}^{V_{FB}^{(1)} + V_p} C^{(1)} dV \qquad \text{(A1)}$$

equals the area under the $C^{(1)}$-$V$ curve shown in Fig. 9. During the voltage pulse, the charge $-\delta Q$ is injected from the silicon and the charge $-Q^{(1)}$ already present in the nitride before the pulse shifts toward the gate. The resulting current flow adds the charge $Q^*$ to the current integrator output (Fig. 10).

The discharge current spike at the termination of the voltage

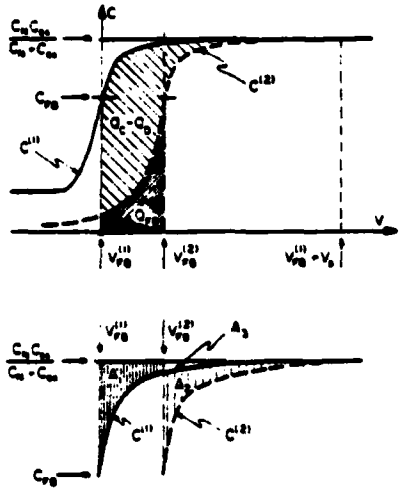

Fig. 9. Capacitance versus voltage before ($C^{(1)}$) and after ($C^{(2)}$) a pulse. Areas under these curves represent the charges flowing through the external circuit during the charging ($Q_C$) and discharging ($Q_D$) spikes (see Fig. 10), and during the restoration of flat band ($Q_{FB}$). Equation (A5) follows from the relation $A_1 + A_3 = A_2 + A_3$ for the areas shown in the enlarged section.

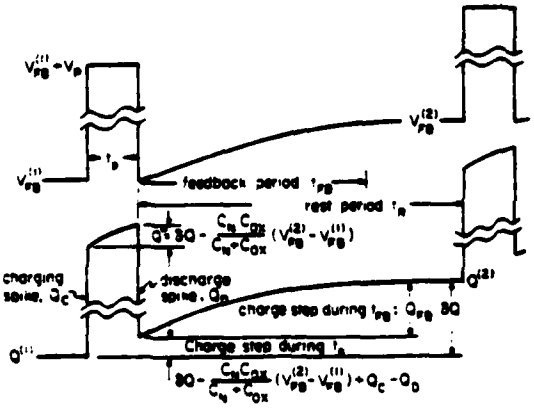

Fig. 10. Voltage across the MNOS device terminals, and charge passed through the external circuit to the gate, neglecting leakage current and retention losses during the rest period.

pulse removes the charge

$$Q_D = \int_{V_{FB}^{(1)}}^{V_{FB}^{(1)} + V_p} C^{(2)}\, dV \tag{A2}$$

from the current integrator. The $C^{(2)}$-$V$ curve shown in Fig. 9 is shifted with respect to the $C^{(1)}$-$V$ curve by the change of flat-band voltage $V_{FB}^{(2)} - V_{FB}^{(1)}$. Portions of the discharge $C^{(2)}$-$V$ curve pertain to "deep depletion," since the short switching-off time of the pulse prevents formation of a hole inversion charge except in cases of small gate width and existence of a lateral source for holes. The device is not at the flat-band voltage of $C^{(2)}$ at the termination of the discharge current spike, but at the bias voltage $V_{FB}^{(1)}$ causing depletion. The charges in the charging and discharging spikes do not cancel since the capacitance is larger when charged than when discharged. The charge registered by the current integrator after the discharge is

$$Q_I = Q^{(1)} + Q_C - Q_D + Q^*. \tag{A3}$$

The charge

$$Q_{FB} = \int_{V_{FB}^{(1)}}^{V_{FB}^{(2)}} C^{(2)}\, dV \tag{A4}$$

is added when the feedback circuit restores flat band, assuming again that $t_{FB}$ is short versus the time required for inversion charge buildup. Fig. 9 shows that

$$Q_C - Q_D + Q_{FB} = \frac{C_{ox} C_N}{C_{ox} + C_N} \left(V_{FB}^{(2)} - V_{FB}^{(1)}\right). \tag{A5}$$

The expressions for $Q^*$ and $Q_1$ listed in Fig. 10 follow from (A3) and (A5), considering that

$$Q^{(2)} - Q^{(1)} = Q_C - Q_D + Q^* + Q_{FB}. \tag{A6}$$

## Acknowledgment

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# Computer-controlled MNOS testing circuit

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**Abstract** A computer-controlled testing circuit for MNOS devices is described. The principal type of test for which the circuit is designed is the stair-case charging method which charges an MNOS device under constant oxide field. Other tests such as memory retention and endurance are also described.

## 1 Introduction

Recently Lehovec *et al* (1978) have described a stair-case charging method for MNOS memory devices which uses a sequence of constant-voltage pulses superimposed on the flat-band voltage pertaining to the previous pulse. This technique has been used by Thornber and Kahng (1978, Thornber *et al* 1978) to study tungsten-doped double-dielectric structures.

In this note a computer-controlled circuit for stair-case charging is described. Use of digital circuits and computer control provides many advantages. Input parameters such as pulse height and duration which are normally manually adjusted with the help of an oscilloscope are now precisely and reproducibly controlled. Measured data such as flat-band voltage and injected charge are digitally stored and can be immediately analysed to produce other information such as charge centroid and injected current. While the circuit was initially developed for the specific purpose of measuring the flat-band voltage and injected charge under constant oxide field conditions the versatility of the system enables one to perform other testing procedures such as memory retention under various initial conditions and endurance tests. Safeguards preventing runaway feedback which can burn out devices have been incorporated into the feedback program.

## 2 Test circuit

The circuit (figure 1) is similar to those described previously (Lehovec *et al* 1978) except that the analogue feedback part has been replaced by digital circuits. The small capacitor $C_c$ in series with the lock-in impedance of 30 pF shunted by 100 MΩ acts as a high-pass filter which blocks most of the stair-case pattern signal, thus eliminating overloading of the lock-in amplifier. The digital circuits consist of a PDP 11/10 central processor unit (CPU), 16 kbytes of core memory and a laboratory peripheral system. The latter includes eight input channels multiplexed to a 12-bit analogue-to-digital converter (ADC) (±5 V), two 12-bit digital-to-analogue converters (DAC) (±5 V), a programmable quartz timer, two Schmitt triggers, two relays and a 6-digit LED display. Because all of the control registers for these devices act as part of the computer memory the devices are under computer control.

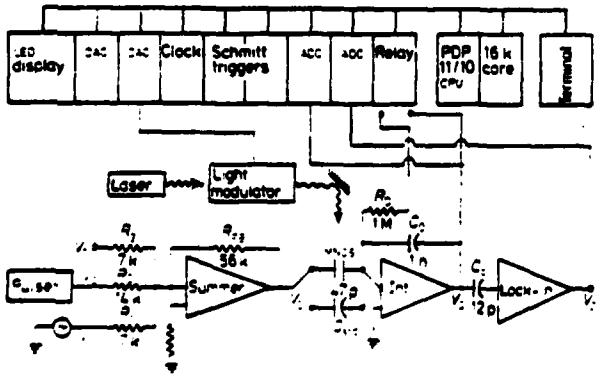


**Figure 1** Computer-controlled testing circuit.

Two analogue-to-digital channels are used to measure voltages $V_C$ and $V_Q$ with a resolution of one voltage bit (2·44 mV). $V_C$ and $V_Q$ are proportional to the MNOS capacitance and charge flowing through the external circuit. One of the digital-to-analogue channels is used to adjust the gate voltage to reach flat-band conditions and to provide the charging pulses. The gate voltage before each pulse is equal to the flat-band voltage and is taken to be the product of the DAC output and the gain of port 3 of the summing amplifier. The duration of the pulses is determined with the help of the programmable clock which can be set to run at frequencies ranging in decades from 1 MHz to 100 Hz. Including the time needed for machine language instruction execution, pulse widths of 20 μs and more can be produced with a resolution of 1 μs. The clock is also used to measure the time intervals between successive capacitance measurements. This interval is set as four times the lock-in time constant. The relay which is in series with the discharging resistor $R_D$ is opened under computer control before each experimental run. The Schmitt triggers can be fired when a signal reaches a predetermined level. Upon firing either the computer is interrupted in order to execute some subroutine or a flag is set. The trigger can be used to synchronise the charging experiment with the triggering of an oscilloscope in order to display $V_G$, $V_C$ or $V_Q$ as a function of time. It can also be used to sense an overload of the lock-in amplifier. A pulse slightly wider than the charging pulse is provided by the second ADC to the acousto-optical modulator to illuminate the MNOS device during the charging pulse. Illumination reduces the recovery time of the silicon space charge capacitance from deep depletion.

## 3 Test technique

The first step in testing a sample is to determine its capacitance-voltage characteristic. This is accomplished by incrementing $V_3$ between two given values and storing the resulting values of $V_C$. The values of the accumulation and depletion capacitances, $C_{acc}$ and $C_{dep}$, determine the flat-band capacitance. When a charging or discharging pulse is applied, the $C$–$V$ curve is shifted horizontally. Flat-band conditions are restored by measuring the change in $V_C$ and adding a voltage $\Delta V_3 = s_L \times \Delta V_C$ to the third input port of the summing amplifier. The derivative $s_L = \partial V_3/\partial V_C|_{V_C=V_{ref}}$ is computed when the $C$–$V$ curve is taken; $V_{ref}$ is the reference voltage which corresponds to the flat-band capacitance. If $V_C$ were a linear function of $V_3$ this procedure would restore flat-band conditions in one step. Figure 2(*a*) shows a flow chart for the subroutine which restores flat-band conditions. This subroutine could be written in a higher-level language but typical execution times would be about 50–100 ms. Being written in machine language, its speed is limited only by the response time (2 ms) of the lock-in amplifier. The variable time interval TL in step 1 is this response time which is set at four times the chosen lock-in time constant. In step 4 the absolute value of the difference $\Delta V_C$ between the measured and the reference voltage $V_{ref}$ is

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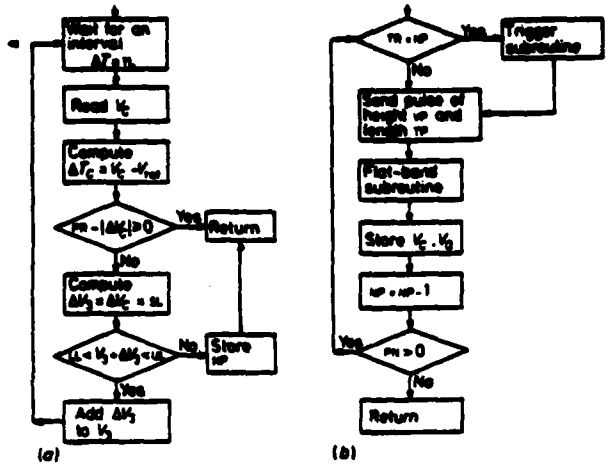


**Figure 2** (*a*) Flow chart for flat-band restoration subroutine. (*b*) Flow chart for pulsing subroutine.

compared to the variable precision PR. If $\Delta V_C$ is smaller than PR then flat-band conditions are considered to be reached within the prescribed precision. There are two criteria for choosing PR. First it should be larger than the noise level at the output of the lock-in. Secondly it should be larger than the capacitance change produced by an increment of $V_3$ of one voltage bit (2·44 mV), i.e. PR > 2·44 mV/SL. The last requirement is usually the limiting one. A typical value of SL is 0·025. This translates into a value of 100 mV for PR and a precision of 2 pF for the capacitance. In step 6 the new computed value of $V_3$ is compared with an upper and a lower limit (UL and LL). This is to prevent a runaway condition applying too high a voltage to the device.

## 4 Pulsing program

The pulsing program (figure 2(*b*)) is written in machine language and can be accessed via a nine-argument function in a higher-level language. The analysis of the data and setting of the parameters is programmed in the higher-level language which uses an interpreter. The nine arguments are: NP, number of pulses; TP, pulse duration in number of clock cycles; VP, pulse height; TR, a pulse number; RP and RL, clock rates to measure the pulse length and the time interval TL between successive readings of $V_C$; PR, precision to which the flat-band voltage is restored; and SL, the previously defined slope. Each time a pulse is sent NP is decremented. When TR = NP a trigger subroutine is executed. This subroutine can be used to send a triggering pulse to an oscilloscope so that the response of $V_C$ or $V_Q$ to a particular pulse can be viewed. This subroutine can be changed to achieve different results such as changing the polarity of the pulses after a certain number of them have been sent. While the subroutine was written to perform a stair-case charging experiment, certain settings of the input parameters will achieve different ends. Setting NP = 1 and VP = 0 results in no pulse being sent and flat-band conditions restored. This is used for the initial gate voltage setting of a device before pulsing and for measuring long-term decay of stored memory charge. Setting PR to a very large value results in no flat-band restoration between pulses. This is used in endurance testing when a large number of pulses of alternating polarity are applied to the device, after which its memory retention and other characteristics are measured. The alternation of polarity is handled by changing the trigger subroutine.

**Acknowledgment**

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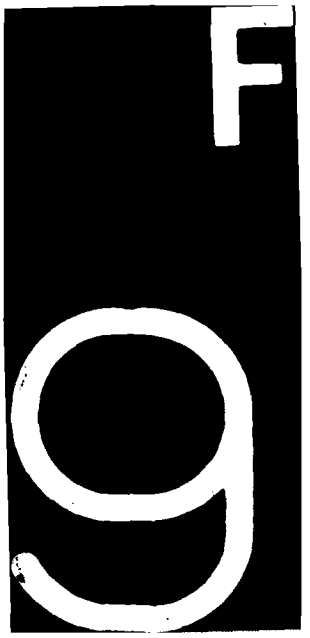
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